Amendments to the Claims

Please amend Claims 1, 5, and 14. Please add new Claims 27-29. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (currently amended) A clock multiplier comprising:

a delay line which provides a multiplied clock having a frequency greater than a reference clock;

a clock multiplexer which applies as an input to the delay line, at respective times, the multiplied clock and [[a]] the reference clock; and

a delay adjustment circuit including a proportional phase comparator which adjusts delay in the delay line based on a direct phase comparison of the reference clock and of the multiplied clock.

2. (original) A clock multiplier as claimed in claim 1 in which the phase comparator has a phase offset of less than five percent of a bit time.

3. (original) A clock multiplier as claimed in claim 1 in which the phase comparator has a phase offset of less than ten percent of a gate time.

4. (original) A clock multiplier as claimed in claim 1 wherein the delay adjustment circuit includes a combined phase comparator and charge pump.

5. (currently amended) A data communications circuit comprising:

a data multiplexing circuit for multiplexing data on a transmission medium; and

a clock multiplier comprising:

a delay line which provides a multiplied clock, having a frequency greater than a reference clock, which is applied back to the input of the delay line; and

a delay adjustment circuit including a phase comparator which adjusts delay in the delay line based on a direct phase comparison of [[a]] the reference clock and the multiplied clock.

6. (original) A data communications circuit as claimed in claim 5 wherein the clock multiplier further comprises a clock multiplexer which applies as an input to the delay line, at respective times, the multiplied clock and the reference clock.

7. (original) The data communications circuit of claim 6 wherein the phase comparator is a proportional phase comparator.

8. (original) A communications circuit as claimed in claim 7 wherein the phase comparator has an offset of less than five percent of a bit time.

9. (original) A communications circuit as claimed in claim 7 in which the phase comparator has a phase offset of less than ten percent of a gate time.

10. (original) A data communications circuit as claimed in claim 7 wherein the delay adjustment circuit includes a combined phase comparator and charge pump.

11. (original) A data communications circuit as claimed in claim 5 which is a data transmitter, the data multiplexing circuit being a data multiplexer.

12. (original) A data communications circuit as claimed in claim 5 which is a receiver, the data multiplexing circuit being a data demultiplexer.

13. (original) A data communications circuit as claimed in claim 5 which is a transceiver and comprising a first multiplexing circuit which is a data multiplexer and a second data multiplexing circuit which is a data demultiplexer.

14. (currently amended) A method of generating a multiplied clock comprising:

applying a reference clock through a clock multiplexer to a delay line;

applying a multiplied clock, having a frequency greater than the reference clock, from the delay line through the clock multiplexer to the input of the delay line; and

in a proportional phase comparator, directly comparing the phase of the reference clock and the multiplied clock; and

adjusting the delay of the delay line based on the phase comparison.

15. (original) A method as claimed in claim 14 wherein the phase comparison has a phase offset of less than five percent of a bit time.

16. (original) A method as claimed in claim 14 as claimed in claim 1 in which the phase comparator has a phase offset of less than ten percent of a gate time.

17. (original) A method as claimed in claim 14 wherein the delay of the delay line is adjusted in a delay adjustment circuit including a combined phase comparator and charge pump

18. (previously presented) A method of communicating data comprising:

applying a delay line output to an input of the delay line to provide a multiplied clock;

directly comparing the phase of the multiplied clock with a reference clock;

adjusting the delay of the delay line based on the phase comparison; and

applying the multiplied clock to a data multiplexing circuit for multiplexing data on a transmission medium.

19. (original) A method as claimed in claim 18 wherein the delay line output is applied to the input of the delay line through a clock multiplexer which applies as an input to the delay line, at respective times, the multiplied clock and reference clock.

20. (original) A method as claimed in claim 19 wherein the phase of the multiplied clock is compared with the reference clock in a proportional phase comparator.

21. (original) A method as claimed in claim 20 wherein the phase comparator has an offset of less than five percent of a bit time.

22. (original) A method as claimed in claim 20 in which the phase comparator has a phase offset of less than ten percent of a gate time.

23. (original) A method as claimed in claim 20 wherein the phase comparator is included in a combined phase comparator and charge pump.

24. (original) A method as claimed in claim 18 wherein the multiplexing circuit is a data multiplexer for transmitting data to the transmission medium.

25. (original) A method as claimed in claim 18 wherein the data multiplexing circuit is a data demultiplexer which receives data from a transmission medium.

26. (original) A method as claimed in claim 18 wherein the data multiplexing circuit is a transceiver including a data multiplexer in a data transmitter and a data demultiplexer in a data receiver.

27. (new) A data communications data transmitter circuit comprising:

a data multiplexer for multiplexing data on a transmission medium; and

a clock multiplier comprising:

a delay line which provides a multiplied clock which is applied back to the input of the delay line; and

a delay adjustment circuit including a phase comparator which adjusts delay in the delay line based on a direct phase comparison of a reference clock and the multiplied clock.

28. (new) A data communications receiver circuit comprising:

a data demultiplexer for demultiplexing data from a transmission medium; and

a clock multiplier comprising:

a delay line which provides a multiplied clock which is applied back to the input of the delay line; and

a delay adjustment circuit including a phase comparator which adjusts delay in the delay line based on a direct phase comparison of a reference clock and the multiplied clock.

29. (new) A data communications transceiver circuit comprising:

a data multiplexer and a data demultiplexer for multiplexing data on a transmission medium; and

a clock multiplier comprising:

a delay line which provides a multiplied clock which is applied back to the input of the delay line; and

a delay adjustment circuit including a phase comparator which adjusts delay in the delay line based on a direct phase comparison of a reference clock and the multiplied clock.